jc932 U.S. PTO
09/656692

09-08-00

A

ASSISTANT COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, DC 20231

PATENT
Date: September 7, 2000
File No. 0941.64727

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): Kenichi Hamada, Satoshi Furuta, Masakazu Taguchi

I hereby certify that this paper is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: Asst. Comm. for Patents, Washington, D.C. 20231, on this date.

9-7-00
Date

Express Mail Label No.: EL409507419US

For: CLOCK ADJUSTMENT APPARATUS FOR A DATA REPRODUCTION SYSTEM AND AN APPARATUS HAVING A DATA . . .

jc836 U.S. PTO
09/656692
09/07/00

Enclosed are:

(X) 37 pages of specification, including 20 claims and an abstract.
(X) an executed oath or declaration, with power of attorney.
( ) an unexecuted oath or declaration, with power of attorney.
( ) ____ sheet(s) of informal drawing(s).
(X) 11 sheet(s) of formal drawings(s).
(X) Assignment(s) of the invention to FUJITSU LIMITED.
(X) Assignment Form Cover Sheet.
(X) A check in the amount of $ 40.00 to cover the fee for recording the assignment(s) is enclosed.
(X) Information Disclosure Statement.
(X) Form PTO-1449 and cited references.
( ) Associate power of attorney.
(X) Priority Document.

Fee Calculation For Claims As Filed

a) Basic Fee								$ 690.00
b) Independent Claims	3	- 3 =	0	x	$ 78.00	=	$	
c) Total Claims	20	- 20 =	0	x	$ 18.00	=	$	
d) Fee for Multiple Claims					$260.00	=	$	
			Total Filing Fee				$	690.00

(X) A check in the amount of $ 690.00 to cover the filing fee is enclosed.

(X) The Commissioner is hereby authorized to charge any additional fees which may be required to this application under 37 C.F.R. §§1.16-1.17, or credit any overpayment, to Deposit Account No. 07-2069. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 07-2069. A duplicate copy of this sheet is enclosed.

Suite 8660 - Sears Tower
233 S. Wacker Drive
Chicago, Illinois 60606
(312) 993-0080

GREER, BURNS & CRAIN, LTD.

By: _____
Patrick G. Burns
Registration No. 29,367

I hereby certify that this paper is being deposited with the United States Postal Service as Express Mail in an envelope addressed to: Asst. Comm. for Patents, Washington, D.C. 20231, on this date.

September 7, 2000
Date

Express Mail Label No.:
EL409507419US

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Kenichi Hamada, a citizen of Japan residing at Kawasaki, Japan, Satoshi Furuta, a citizen of Japan residing at Kawasaki, Japan and Masakazu Taguchi, a citizen of Japan residing at Kawasaki, Japan have invented certain new and useful improvements in

CLOCK ADJUSTMENT APPARATUS FOR A DATA REPRODUCTION SYSTEM AND AN APPARATUS HAVING A DATA REPRODUCTION SYSTEM INCLUDING SUCH A CLOCK ADJUSTMENT APPARATUS

of which the following is a specification : -

TITLE OF THE INVENTION

CLOCK ADJUSTMENT APPARATUS FOR A DATA REPRODUCTION SYSTEM AND AN APPARATUS HAVING A DATA REPRODUCTION SYSTEM INCLUDING SUCH A CLOCK ADJUSTMENT APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to clock adjustment apparatus for data reproduction systems and apparatus having data reproduction systems including such clock adjustment apparatus, and more particularly, to a clock adjustment apparatus for a data reproduction system of a data recording apparatus such as an optical disk apparatus, a magneto-optical disk apparatus or a magnetic disk apparatus, and an apparatus having a data reproduction system including such a clock adjustment apparatus. A magneto-optical disk apparatus, for example, requires an increasingly high recording density of a recording medium, and therefore, needs a data recording/reproduction method with higher accuracy. Adopted as one of such methods is a combination of recording data modulated to a partial response (PR) waveform onto a magneto-optical disk and sampling a readout signal from the magneto-optical disk at a predetermined sampling frequency so as to detect maximum likelihood data through, what is called, the Viterbi decoding detection (or the maximum likelihood sequence estimation: MLSE). Hereinafter, this combination method is referred to as a PRML method.

With respect to the PRML method, it is important to provide phase compensation so that a quantized readout signal can be sampled in synchronism with a clock signal.

2. Description of the Related Art

Regarding a data reproduction system for reproducing recorded data in accordance with the Viterbi algorithm from sampled values obtained by sampling readout data from a recording medium in synchronism with a clock signal, it is necessary to adjust the phase of the clock signal so that the best sampled values can be obtained.

A conventional clock adjustment apparatus for the data reproduction system estimates the phase error of the clock signal by using a value (for example, a center value of the readout signal) calculated in the process of reproducing recorded data through the Viterbi algorithm so as to control the phase of the clock signal by using the phase error.

According to such a conventional clock adjustment apparatus, the overall structure of the data reproduction system including the clock adjustment apparatus can be simplified.

On the other hand, the above-described data reproduction system requires a higher-speed clock signal because of a higher recording density of the recording medium.

However, the conventional clock adjustment apparatus, which estimates the phase error of the clock signal by using the processed readout data through the Viterbi algorithm, has difficulty in obtaining such a higher-speed clock signal necessary to guarantee the sampling of the readout signal at the right phase.

SUMMARY OF THE INVENTION

It is a general object of the present invention to provide a clock adjustment apparatus for a data reproduction system and an apparatus having a data reproduction system including such a clock adjustment apparatus in which the above

disadvantages are eliminated.

A more specific object of the present invention is to provide a clock adjustment apparatus for a data reproduction system, which clock adjustment apparatus produces a clock signal fast enough to guarantee sampling of a readout signal at the right phase, and an apparatus having a data reproduction system including such a clock adjustment apparatus.

The above-mentioned objects of the present invention are achieved by a clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, the recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, the clock adjustment apparatus including a phase error calculation circuit calculating the phase error of the clock signal based on the sampled values of the readout signal.

According to the above-mentioned data reproduction system, the waveform of the readout signal from the recording medium depends on the predetermined PR characteristic. When such a readout signal is sampled in synchronism with the clock signal of the right phase, the transition state of the sampled values also depends on the PR characteristic. Therefore, the phase error of the clock signal can be obtained based on the extent of the difference between the transition state of the sampled values obtained in synchronism with the clock signal and the transition state of expected sampled values corresponding to the PR

characteristic.

The above-mentioned objects of the present invention are also achieved by a clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, the recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, the clock adjustment apparatus including a phase error calculation circuit calculating the phase error of the clock signal based on a transition state of the sampled values of the readout signal before undergoing the Viterbi algorithm.

The above-mentioned objects of the present invention are further achieved by an apparatus including a data reproduction system which samples a readout signal from a recording medium in synchronism with a clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, the data reproduction system having a clock adjustment circuit including a phase error calculation circuit calculating a phase error of the clock signal based on the sampled values of the readout signal, and adjusting a phase of the clock signal based on the phase error.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects, features and advantages of

the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram showing a structure of an optical disk apparatus according to an embodiment of the present invention;

FIG. 2 is a block diagram showing a structure of a readout system unit of the optical disk apparatus of FIG. 1;

FIG. 3 is a block diagram showing a structure of a phase error detection unit of the readout system unit of FIG. 2;

FIG. 4 is a block diagram showing a structure of a phase error detection circuit of the phase error detection unit of FIG. 3;

FIG. 5 is a diagram showing a waveform of a readout signal before being supplied to a Viterbi detection module so as to illustrate a phase error determined from an equation;

FIG. 6 is a diagram for illustrating a threshold defined so as to prevent a wrong portion of the readout signal from being detected as an edge portion;

FIG. 7 is a diagram for illustrating a masking threshold;

FIG. 8 is a block diagram showing a structure of an edge detection circuit of the phase error detection unit of FIG. 3;

FIG. 9 is a diagram showing a convergence process of the phase error of a clock signal according to the present embodiment;

FIG. 10 is a timing chart illustrating a switching of sampled values of the readout signal employed to detect the phase error; and

FIG. 11 is a diagram illustrating normalization of a phase error output.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A description will now be given, with reference to the accompanying drawings, of an embodiment of the present invention.

FIG. 1 shows a structure of an optical disk apparatus according to the embodiment of the present invention. The optical disk apparatus is a magneto-optical disk apparatus employing a magneto-optical disk as a recording medium.

According to FIG. 1, the magneto-optical disk apparatus includes a magneto-optical disk 10 serving as a recording medium, an optical head 20, an amplifier 21, a readout system unit 25, a writing system unit 26, an electromagnet 27, a control unit (MPU) 28, a servo system unit 29, and a motor 30. Data is recorded on the magneto-optical disk 10 in accordance with the recording rule of a predetermined PR characteristic (for example, the PR (1, 1) of a constraint length 2), and is reproduced from the magneto-optical disk 10.

The MPU 28 controls the readout system unit 25, the writing system unit 26 and the servo system unit 29 in accordance with a data readout command and a data writing command provided from an external unit (not shown) through a connector 32 and an interface circuit 31. A description will be given later of the control of the MPU 28 over the readout system unit 25.

According to the above-described magneto-optical disk apparatus, the optical head 20 optically scans the magneto-optical disk 10 when the data readout command is provided thereto, so that a readout signal output from the optical head 20 is provided to the readout system unit 25 through the amplifier 21. The readout system unit 25 quantizes the provided readout signal and generates output

data from the quantized data in accordance with a maximum likelihood (ML) decoding algorithm (for example, the Viterbi algorithm). The output data is provided to the MPU 28 and is further output therefrom to the external unit through the interface circuit 31 and the connector 32.

On the other hand, when the MPU 28 receives the data writing command as well as data to be recorded from the external unit, the MPU 28 modulates the data in accordance with the predetermined recording rule (for example, the PR (1, 1)), and provides the modulated data to the writing system unit 26. The writing system unit 26 controls the operation of the optical head 20 in accordance with the modulated data, and the MPU 28 controls the electromagnet 27 in accordance with data obtained from the modulation of the data. As a result, the data is written on the magneto-optical disk 10 in accordance with the above-mentioned predetermined recording rule.

The servo system unit 29, which is controlled by the MPU 28, actuates the motor 30 so as to rotate the magneto-optical disk 10 at a predetermined speed, and positions the optical head 20 at the recording/reproduction position of the magneto-optical disk 10.

FIG. 2 shows a structure of the above-described readout system unit 25.

According to FIG. 2, the readout system unit 25 includes a low-pass filter (LPF) 22, an analog-to-digital converter (ADC) 23, a digital equalizer (EQ) 24, a Viterbi detection module 100, and a clock generation circuit 200.

The readout signal amplified by the amplifier 21 shown in FIG. 1 is subjected to waveform shaping at the LPF 22. The analog readout signal output by the LPF 22 is sampled periodically

by the ADC 23. The ADC 23 converts the readout signal into a digital-form readout signal in synchronism with a clock signal supplied from the clock generation circuit 200. In other words, the above-mentioned readout signal is quantized by being sampled by the ADC 23 operating in synchronism with the clock signal.

The ADC 23 continuously samples the readout signal in synchronism with the clock signal generated from the clock generation circuit 200, and outputs the digitized readout signal. The EQ 24 performs waveform equalization on the sampled values of the digitized readout signal, so that the sampled values are output as equalized output data (quantized data). The equalized output data from the EQ 24 is provided to the Viterbi detection module 100 in synchronism with the above-mentioned clock signal. The Viterbi detection module 100 detects, in accordance with the Viterbi algorithm, the recorded data from the equalized output data provided in synchronism with the clock signal, and outputs the recorded data as reproduced data. In the data reproduction system of FIG. 1, the EQ 24 and the Viterbi detection module 100 also operate in synchronism with the clock signal supplied by the clock generation circuit 200, although this is not indicated in FIGS. 1 and 2.

Like generally used Viterbi detectors, the above-mentioned Viterbi detection module 100 includes a branch metric calculation unit (BM) 101, an add-compare-select unit (ACS) 102, a path metric memory (PMM) 103, and a path memory (PM) 104.

The BM 101 calculates branch metrics which corresponds to the differences between sampled values and expected values which the readout signal should take depending on the PR characteristic. The ACS 102 adds previously calculated path metrics

stored in the PMM 103 to the corresponding above-mentioned branch metrics. The ACS 102 then compares each given pair of the calculated path metrics so as to select the smaller of the two. The selected path metrics are stored in the PMM 103 as new path metrics. According to the above-described calculation, a path metric is expressed as an addition of branch metrics.

Selecting the smaller path metric as described above corresponds to selecting a state transition path in the Viterbi algorithm. That is to say, the ACS 102 always selects a path so as to minimize the path metric. The ACS 102 supplies the PM 104 with binary data corresponding to the path selected in the above-described way. In the PM 104 data corresponding to each of the selected paths is shifted, while discarding data corresponding to each of non-selected paths. As a result, data corresponding to each of the surviving paths is output from the PM 104 as output data. Thus, the data recorded with high density on the magneto-optical disk 10 can be reproduced with high accuracy by recording the data in a PR waveform and detecting the maximum likelihood data by the Viterbi detection module 100.

The above-mentioned clock generation circuit 200, serving as a feedback loop, includes a phase error detection unit (PED) 230 serving as a means for detecting a phase error, a digital-to-analog converter (DAC) 240 and a phase-locked loop (PLL) 250.

As will be described later, the PED 230 detects the phase error of the above-mentioned clock signal on the basis of the sampled values of the digitized readout signal obtained before undergoing the Viterbi detection module 100. First sampled values S1, which are quantized by the ADC 23 but not

subjected to the waveform equalization performed by the EQ 24, and second sampled values S2, on which the waveform equalization is performed by the EQ 24, are provided to the PED 230 in order to detect the phase error of the clock signal.

The phase error of the clock signal detected by the PED 230 is converted into a corresponding voltage level (an analog value) by the DAC 240. The PLL 250, which includes a loop filter (LF) and a voltage-controlled oscillator (VCO), controls the phase of the clock signal so as to reduce the phase error, based on the corresponding voltage level provided from the DAC 240. The clock signal, of which the phase is adjusted by the PLL 250, is provided to the ADC 23 sampling the readout signal.

FIG. 3 is a block diagram showing a structure of the PED 230 shown in FIG. 2. Also shown in FIG. 3 is the above-described MPU 28 inputting a plurality of control signals to the PED 230.

The PED 230 operates in two detection (operation) modes, namely, an acquisition mode and a tracking mode, to detect the phase error of the clock signal. The acquisition mode is an initial adjustment mode, where the phase of the clock signal is adjusted, by using a VFO region arranged on a leading portion of each of the tracks of the magneto-optical disk 10, so that the sampling of the readout signal is properly performed. In the acquisition mode, it is preferable to adjust the phase of the clock signal quickly by setting a gain to a high (Hi) state. A continuous repeat pattern modulated in accordance with the PR characteristic is recorded on the above-mentioned VFO region, and the phase error of the clock signal can be reduced by adjusting the phase thereof in accordance with

the repeat pattern.

On the other hand, in the tracking mode, the phase error is gradually controlled by setting the gain to a low (Low) state after the phase of the clock signal is adjusted in the acquisition mode to reduce the phase error. The tracking mode is employed in a data recording (DATA) region, on which is recorded a data signal obtained by modulating desired data in accordance with the PR characteristic.

The PED 230 includes a multiplexer (MUX) 231, a phase error detection (calculation) circuit 233, an edge detection circuit 235, an OR circuit 236, an AND circuit 237, a gain adjustment circuit 238, and an AND circuit 239. The PED 230 detects the phase error of the clock signal in accordance with the control signals input from the MPU 28.

The first and second sampled values S1 and S2 output successively after being digitized in the ADC 23 and equalized in the EQ 24, respectively, are input to the MUX 231. The MPU 28 inputs a sampled value selection signal 40 to the MUX 231 so that the MUX 231 outputs the first sampled values S1 in the acquisition mode and the second sampled values S2 in the tracking mode. In the tracking mode, by employing the equalized second sampled values S2, the phase error of the clock signal can be calculated based on the sampled values of the readout signal having a waveform closer to that to be reproduced. The MPU 28 inputs to the OR circuit 236 a mode selection signal 42 "1" when the phase error is output at all the sampling instants and a mode selection signal 42 "0" when the phase error is output only at edge portions of the data signal. Thus, the MPU 28 serves as an operation mode switching circuit.

The phase error detection circuit 233

calculates the phase error of the clock signal in accordance with a below-described predetermined calculation process in the acquisition and tracking modes, and outputs a corresponding signal to the AND circuit 237. The edge detection circuit 235 detects a rising edge portion or a falling edge portion of the recorded data of the readout signal in the tracking mode, and outputs a corresponding signal, which is input to the AND circuit 237 via the OR circuit 236.

The output signals from the phase error detection circuit 233 and the edge detection circuit 235 are supplied to the AND circuit 237. The AND circuit 237 produces an output signal corresponding to the supplied signals, and outputs the corresponding signal to the gain adjustment circuit 238. At this point, the MPU 28 inputs a gain setting signal 44 to the gain adjustment circuit 238 so that the gain is set to the Hi state in the case of the acquisition mode and to the Low state in the case of the tracking mode. That is, the MPU 28 switches the states of the gain, serving as a gain switching circuit.

The PED 230 generally operates as follows. First, in the acquisition mode, the first sampled values S1 are input to the phase error detection circuit 233 via the MUX 231. The phase error detection circuit 233 calculates the phase error of the clock signal from the first sampled values S1 in accordance with the predetermined calculation process, and outputs the corresponding signal to the AND circuit 237. At the same time, the output signal from the MUX 231 is also supplied to the edge detection circuit 235. Since the mode selection signal 42 "1" is continuously input from the MPU 28 to the OR circuit 236 in the acquisition mode, the output signal from the phase error detection circuit

233 is input to the gain adjustment circuit 238 through the AND circuit 237 in the acquisition mode. In other words, the phase error of the clock signal is continuously detected based on the successive sampled values obtained at the upper peaks (the maximum values), the lower peaks (the minimum values), the rising edge portions, the falling edge portions, and the center points between the upper and lower peaks of the readout signal having the highest density. Therefore, the phase error is so frequently obtained that the phase of the clock signal can be adjusted more quickly. The output signal from the AND circuit 237 is adjusted to have the gain set to the Hi state (hereinafter a Hi gain) by the gain adjustment circuit 238, and is output therefrom as the phase error.

The signal output from the gain adjustment circuit 238 as the phase error is supplied to the DAC 240 shown in FIG. 2 via the AND circuit 239. The AND circuit 239 is controlled by a masking signal 46 output from the MPU 28, which will be described later. When a low-level masking signal is supplied to the AND circuit 239, the signal output from the gain adjustment circuit 238 as the phase error is masked and is not provided to the DAC 240.

On the other hand, in the tracking mode, the second sampled values S2 are input to the phase error detection circuit 233 as well as to the edge detection circuit 235 through the MUX 231. The phase error detection circuit 233 calculates the phase error of the clock signal from the second sampled values S2 in accordance with the predetermined calculation process, and outputs the corresponding signal to the AND circuit 237. The edge detection circuit 235 performs a predetermined edge detection process, which will be described later, on the second sampled values S2. The edge

detection circuit 235 outputs an edge detection signal "1" when determining that the second sampled values S2 are sampled at edge portions of the readout signal, and, when not, outputs an edge detection signal "0". The detection signal is supplied to the OR circuit 236, to which the mode selection signal 42 "0", which indicates that the PED 230 is in the tracking mode, is input from the MPU 28. Therefore, when the edge detection signal "1" is supplied to the OR circuit 236, the output signal from the phase error detection circuit 233 passes through the AND circuit 237 and is output to the gain adjustment circuit 238. Thus, the phase error of only the edge portions of the readout signal is supplied to the gain adjustment circuit 238. The output signal from the AND circuit 237 is adjusted to have the gain set to the Low state (hereinafter a Low gain) by the gain adjustment circuit 238, and is output therefrom. The Low gain is smaller than the Hi gain.

By thus adjusting the gain with respect to the phase error calculated by the phase error detection circuit 233 in accordance with the gain setting signal 44 from the MPU 28, the phase of the clock signal can be adjusted so as to quickly shift close enough to its right phase in the acquisition mode and to be stable without oscillation in the tracking mode.

A description will now be given, with reference to the accompanying drawings, of the calculation of the phase error of the clock signal performed by the phase error detection circuit 233. FIG. 4 is a block diagram showing a structure of the phase error detection circuit 233.

Suppose in FIG. 4 that a first sampled value Y_t at a sampling instant t, a second sampled value Y_{t-1} at a sampling instant t-1, which is

previous to the sampling instant t, and a third sampled value Y_{t-2} at a sampling instant t-2, which is previous to the sampling instant t-1, are input in the order sampled to the phase error detection circuit 233.

The phase error detection circuit 233 includes flip-flops (FF) 331 and 332, subtracters 333, 334 and 339, code determination circuits 335 and 336, and multipliers 337 and 338. The sampled values Y_{t-1} and Y_{t-2} are simultaneously set in the FFs 331 and 332, respectively when the sampled value Y_t is detected at the sampling instant t.

The phase error detection circuit 233 calculates the phase error (PE) of the clock signal based on the following equation:

$$PE = (Y_t - Y_{t-1}) \times hat_{t-1,\ t-2} - (Y_{t-1} - Y_{t-2}) \times hat_{t,\ t-1}$$

where $hat_{t,\ t-1} = 1, 0, -1$ in the cases of $Y_t - Y_{t-1} > 0$, $Y_t - Y_{t-1} = 0$, $Y_t - Y_{t-1} < 0$, respectively, and $hat_{t-1,\ t-2} = 1, 0, -1$ in the cases of $Y_{t-1} - Y_{t-2} > 0$, $Y_{t-1} - Y_{t-2} = 0$, $Y_{t-1} - Y_{t-2} < 0$, respectively.

Since the waveform of the sampled readout signal has the upper and lower peaks, and the center points therebetween, the above equation is provided with a ternary code "hat" to correct the transition direction of the waveform so that the proper phase error can be detected at any of the above points.

The first sampled value Y_t and the second sampled value Y_{t-1} set in the FF 331 are input to the subtracter 333, which subtracts Y_{t-1} from Y_t to calculate a first difference. At the same time, the second sampled value Y_{t-1} set in the FF 331 and the third sampled value Y_{t-2} set in the FF 332 are input to the subtracter 334, which subtracts Y_{t-2} from Y_{t-1} to calculate another first difference. The first

difference calculated by the subtracter 333 is output to the code determination circuit 335. The code determination circuit 335 determines the ternary code for the first difference calculated by the subtracter 333, or determines $hat_{t, t-1}$, and outputs $hat_{t, t-1}$ to the multiplier 338. Simultaneously, the first difference calculated by the subtracter 334 is output to the code determination circuit 336. The code determination circuit 336 determines the ternary code for the first difference calculated by the subtracter 334, or determines $hat_{t-1, t-2}$, and outputs $hat_{t-1, t-2}$ to the multiplier 337. The product of $Y_t - Y_{t-1}$ and $hat_{t-1, t-2}$ calculated by the multiplier 337 and the product of $Y_{t-1} - Y_{t-2}$ and $hat_{t, t-1}$ calculated by the multiplier 338 are output to the subtracter 339. The subtracter 339 finally determines the phase error of the clock signal from the above equation. In other words, the subtracter 339 uses the absolute values of the two first differences, which are calculated by multiplying each of the two first differences by the ternary code "hat" to correct the transition direction, so as to calculate the difference between the two absolute values from the above equation (a second difference), which is equal to the phase error of the clock signal.

FIG. 5 shows a waveform of a readout signal R before being supplied to the Viterbi detection module 100 so as to illustrate the phase error determined from the above equation. The readout signal R is sampled in synchronism with the clock signal to provide sampled values Y. The ideal sampling of the readout signal R is performed by generating the clock signal at the sampling instants t, t-1 and t-2 corresponding to the lower peak, the center point and the upper peak, respectively, of the waveform, shown circled in FIG. 5. If the

readout signal R is sampled at the ideal sampling instants t, t-1 and t-2, the phase error (PE) is given by the above formula as follows:

$$PE = (Y_t - Y_{t-1}) \times hat_{t-1,\,t-2} - (Y_{t-1} - Y_{t-2}) \times hat_{t,\,t-1}$$
$$= (-1) \times (-1) - (-1) \times (-1)$$
$$= 1 - 1$$
$$= 0$$

Thus, it can be confirmed that there exists no phase error.

Next, a description will be given of a case where a phase error exists using FIG. 5. The sampling of the readout signal is performed by generating the clock signal at the sampling instants T, T-1 and T-2, which deviate from the lower peak, the center point and the upper peak, respectively. The waveform is marked with a triangle at each of the sampling instants T, T-1 and T-2.

Suppose that $Y_T = 0.1$, $Y_{T-1} = 0.7$ and $Y_{T-2} = 1.9$, the phase error (PE) is given by the above equation as follows:

$$PE = (Y_t - Y_{t-1}) \times hat_{t-1,\,t-2} - (Y_{t-1} - Y_{t-2}) \times hat_{t,\,t-1}$$
$$= (0.1 - 0.7) \times (-1) - (0.7 - 1.9) \times (-1)$$
$$= 0.6 - 1.2$$
$$= -0.6$$

It is concluded from the above calculation result that the clock signal lags behind by the phase error of 0.6. Consequently, the phase of the clock signal is controlled so as to correct the above phase error. According to the above example, the phase error is calculated with respect to the

falling edge portion including the center point. On the other hand, the phase error can also be calculated with respect to a rising edge portion including a center point, or to an edge portion including an upper or a lower peak. The first differences Y_t-Y_{t-1} and $Y_{t-1}-Y_{t-2}$, that is, the differences between the real sampled values, are multiplied by the ternary codes $hat_{t-1, t-2}$ and $hat_{t, t-1}$, respectively, to correct the transition direction. As a result, the absolute values of the first differences are determined so that the phase error can correctly be calculated based on the first differences irrespective of the sampling instants at which the readout signal is sampled. The difference of the absolute values of the first differences is determined from the above equation as the second difference, which is employed as the phase error to control the phase compensation.

A description will now be given, with reference to FIGS. 6 through 8, of the edge detection in the tracking mode performed by the edge detection circuit 235. The edge detection is provided in order to prevent the phase of the clock signal from shifting from that of the readout signal at the edge portions thereof when the readout signal is reproduced from a storage medium which is likely to cause the distortion of the waveform of the readout signal at the edge portions thereof. The edge detection circuit 235 detects the rising edge portions or the falling edge portions based on the sampled values obtained in the order sampled. Just as previously described, suppose that the first, second and third sampled values Y_t, Y_{t-1} and Y_{t-2} are obtained at the sampling instants t, t-1 and t-2, respectively. The conditions for detecting the rising edge portions are established as $Y_{t-1}-Y_{t-2} > 0$ and $Y_t-Y_{t-1} > 0$.

Since the readout signal sampled in the tracking mode is a data signal, a wrong portion of the readout signal may be detected as an edge portion because of the variation in the recorded data thereof. Therefore, it is preferable to define a threshold T so as to prevent a wrong portion of the readout signal from being detected as an edge portion. In the case of the rising edge portions, the detection of a wrong portion can be precluded by setting the following conditions: the third sampled value Y_{t-2} is smaller than the threshold T ($Y_{t-2} < T$) and the first sampled value Y_t is larger than the threshold T ($Y_t > T$). Under these conditions, FIG. 6 (a) is detected as a rising edge portion, while FIG. 6 (b) and (c) are not. The threshold T is defined, for example, by a control signal from the MPU 28 serving as a threshold defining circuit. The MPU 28 suitably defines the threshold T depending on a type of storage medium. By thus setting the conditions, the rising edge portions of the readout signal can be detected based on a series of discrete but successive sampled values in ascending order from a value smaller than the threshold T to a value larger than the threshold T.

Similarly, the conditions for preventing the detection of a wrong portion can be established with respect to the falling edge portions. In the case of the falling edge portions, the conditions are opposite to those in the case of the rising edge portions. In other words, the conditions are set as follows: $Y_{t-1}-Y_{t-2} < 0$ and $Y_t-Y_{t-1} < 0$, and the third sampled value Y_{t-2} is larger than the threshold T ($Y_{t-2} > T$) and the first sampled value Y_t is smaller than the threshold T ($Y_t < T$).

Further, an asymmetric waveform should be considered in the case of detecting edge portions of a data signal. For example, a waveform of sampled

values of a data signal shown in FIG. 7 (a) includes oval-circled portions each including three successive sampled values. In this case, each of the oval-circled portions can be detected as a falling edge portion based on the above conditions for preventing the wrong detection. If detected in this way, pairs of successive falling edge portions are indicated in a waveform indicating the edge portions of the data signal as shown in FIG. 7 (b). In order to prevent this, it is preferable to perform a masking where a difference between two successive sampled values is masked if the absolute value thereof is smaller than a given value (defined as a masking threshold mT). The masking threshold mT can be defined, for example, based on a control signal from the MPU 28.

A preferred waveform indicating the edge portions of the data signal as shown in FIG. 7 (c) is obtained by masking the first difference $Y_{t-1}-Y_{t-2}$ if $| Y_{t-1}-Y_{t-2} | < mT$ or the first difference $Y_{t}-Y_{t-1}$ if $| Y_{t}-Y_{t-1} | < mT$.

The threshold T is normally a fixed value defined by the MPU 28. In some cases, a data signal is offset in its amplitude direction by the envelope variation thereof caused by the eccentricity of a disk-shaped storage medium. Therefore, it is preferable to perform the edge detection by adding to the threshold T an estimated offset of the data signal caused by the envelope variation thereof or the like. In other words, it is desirable to add, by an adder, the offset estimated by an offset estimation circuit to the threshold T and input the adding result thereof to the edge detection circuit 235. Thereby, the envelope variation of the data signal can be considered in the edge detection, and the threshold T is corrected in accordance with the offset and can be maintained at the best level for

the edge detection.

FIG. 8 shows a structure of the edge detection circuit 235, wherein the threshold T and the masking threshold mT are defined with the offset being considered.

According to FIG. 8, the edge detection circuit 235 includes flip-flops (FF) 351 and 352, an offset estimation circuit 353, an adder 354, and subtracters 356 and 357. The sampled values Y_{t-1} and Y_{t-2} are simultaneously set in the FFs 351 and 352, respectively when the sampled value Y_t is detected at the sampling instant t. The edge detection circuit 235 further includes comparators 361 through 364 and AND circuits 375 and 377 for detecting a rising edge portion, absolute value calculation circuits 371 and 372, comparators 373 and 374, and comparators 365 through 368 and AND circuits 376 and 378 for detecting a falling edge portion.

A description will now be given of the detection of the rising edge portions. The detection of the falling edge portions is performed in the same process as the detection of the rising edge portions by reversing almost all the conditions for the detection of the rising edge portions. Therefore, a detailed description thereof will be omitted.

First, the first sampled value Y_t and the second sampled value Y_{t-1} set in the FF 351 are input to the subtracter 356, and at the same time, the second sampled value Y_{t-1} set in the FF 351 and the third sampled value Y_{t-2} set in the FF 352 are input to the subtracter 357. The calculation result by the subtracter 356 is output to the comparator 361, which determines whether $Y_t - Y_{t-1} > 0$. If $Y_t - Y_{t-1} > 0$, a value "1" is output to the AND circuit 375. If $Y_t - Y_{t-1} \leqq 0$, a value "0" is output to the AND circuit 375. Simultaneously, the calculation result

of the subtracter 357 is output to the comparator 362, which determines whether $Y_{t-1}-Y_{t-2} > 0$. If $Y_{t-1}-Y_{t-2} > 0$, the value "1" is output to the AND circuit 375. If $Y_{t-1}-Y_{t-2} \leqq 0$, the value "0" is output to the AND circuit 375. That is, a portion of the data signal including the above sampled values is detected as a probable rising edge portion when both of the comparators 361 and 362 output the values "1" to the AND circuit 375.

Next, it is determined whether the first and third sampled values Y_t and Y_{t-2} are above and below the threshold T defined by the MPU 28, respectively. The first sampled value Y_t and the threshold T defined by the MPU 28 are input to the comparator 363. At this point, if the data signal has an offset, the threshold T defined by the MPU 28 is corrected by adding, by the adder 354, the offset estimated by the offset estimation circuit 353 thereto and the corrected threshold T is input to the comparator 363. The comparator 363 compares the first sampled value Y_t and the threshold T. The comparator 363 outputs the value "1" to the AND circuit 375 if $Y_t > T$ and the value "0" if $Y_t < T$.

At the same time, the comparator 364 compares the third sampled value Y_{t-2} and the threshold T. The comparator 364 outputs the value "1" to the AND circuit 375 if $Y_{t-2} < T$ and the value "0" if $Y_{t-2} > T$. That is, the portion of the data signal including the above-mentioned sampled values is detected as a probable rising edge portion when both of the comparators 363 and 364 output the values "1" to the AND circuit 375.

Next, a decision is made on the necessity of the masking based on the masking threshold mT defined by the MPU 28. The calculation result of the subtracter 356 is also input to the absolute value calculation circuit 371. The absolute value

$|Y_t-Y_{t-1}|$ calculated by the absolute value calculation circuit 371 and the masking threshold mT defined by the MPU 28 are input to the comparator 373. The comparator 373 compares $|Y_t-Y_{t-1}|$ and the masking threshold mT. The comparator 373 outputs the value "1" to the AND circuit 375 if $|Y_t-Y_{t-1}| > mT$ and the value "0" if $|Y_t-Y_{t-1}| \leqq mT$. Therefore, if $|Y_t-Y_{t-1}| \leqq mT$, the first difference Y_t-Y_{t-1} is masked and the portion of the data signal including the above-mentioned sampled values is not detected as a rising edge portion. Simultaneously, the calculation result of the subtracter 357 is also input to the absolute value calculation circuit 372. The absolute value $|Y_{t-1}-Y_{t-2}|$ calculated by the absolute value calculation circuit 372 and the masking threshold mT defined by the MPU 28 are input to the comparator 374. The comparator 374 compares $|Y_{t-1}-Y_{t-2}|$ and the masking threshold mT. The comparator 374 outputs the value "1" to the AND circuit 375 if $|Y_{t-1}-Y_{t-2}| > mT$ and the value "0" if $|Y_{t-1}-Y_{t-2}| \leqq mT$. Therefore, if $|Y_{t-1}-Y_{t-2}| \leqq mT$, the first difference $Y_{t-1}-Y_{t-2}$ is masked and the portion of the data signal including the above-mentioned sampled values is not detected as a rising edge portion.

The AND circuit 375, to which the above input signals are transmitted, outputs the value "1" to the AND circuit 377 only when all the input signals are the value "1", which indicates that the portion of the data signal including the above-mentioned sampled values is detected as a rising edge portion. In the case of selecting a rising edge portion, the MPU 28 supplies a rising edge selection signal "1" to the AND circuit 377, which outputs a corresponding signal to an OR circuit 379.

The detection of the falling edge portions proceeds similarly through the comparators 365

through 368, the absolute value calculation circuits 371 and 372, the comparators 373 and 374, and the AND circuit 376. In the case of selecting a falling edge portion, the MPU 28 supplies a falling edge selection signal "1" to the AND circuit 378, which outputs a corresponding signal to the OR circuit 379. Therefore, when a rising or a falling edge portion is detected, the OR circuit outputs the edge detection signal. In other words, the edge detection circuit 235 shown in FIG.3 outputs the edge detection signal "1" to the OR circuit 236.

FIG. 9 shows a convergence process of the phase error of the clock signal according to the present embodiment. A waveform 400 indicates the output level of the phase error. The MPU 28 determines a timing for switching the acquisition and tracking modes by making a judgment on the state of convergence of the phase error of the clock signal. The timing can be determined depending on the characteristic of a storage medium by the MPU 28 serving as a convergence time setting circuit. The convergence of the phase error is determined when the amplitude of a detected phase error output remains within a predetermined range for a predetermined period of time, namely, for a longer period than a predetermined reference time length set by the MPU 28. The MPU 28 functioning as a convergence range setting circuit can also set the predetermined range. The acquisition mode can smoothly be switched to the tracking mode after it is determined that the phase error converges within the predetermined range according to the above judgment on the convergence state thereof.

As the MPU 28 can make the above judgment on the convergence state of the phase error, the MPU 28 can automatically switch the acquisition mode to the tracking mode by outputting the mode selection

signal 42 to the OR circuit 236 when the convergence of the phase error within the predetermined range is determined. Further, the gain setting signal 44 input to the gain adjustment circuit 238 from the MPU 28 can be set so as to automatically switch the state of the gain from Hi to Low, simultaneously with the above-mentioned mode switching, after the convergence of the phase error within the predetermined range is confirmed. A dotted waveform 410 in FIG. 9 shows a waveform which the phase error takes if the gain is maintained in the original state, that is, the Hi state, without being switched to the Low state. As can be seen from the comparison between the waveform 400 and the dotted waveform 410, the range of the amplitude of the phase error narrows faster with the Low gain than the Hi gain after the convergence of the phase error within the predetermined range is determined.

In FIG. 9, the predetermined range of the amplitude of the phase error is set between a first output level H and a second output level L. When the amplitude of the phase error detected by the phase error detection circuit 233 falls within the above-mentioned predetermined range, a timer operation is started to count the time length required for the phase error to shift between the first and second output levels H and L. When the time length is shorter than a reference time length, the mode switching does not occur. On the other hand, when the time length is longer than the reference time length, the mode switching occurs. For example, in the case of a time length C1 in FIG. 9, which is shorter than a predetermined reference time length C, the mode switching does not occur and the acquisition mode is maintained. On the other hand, in the case of a time length C2, which is longer than the predetermined reference time length

C, the mode is switched from the acquisition mode to the tracking mode and the state of the gain is switched from Hi to Low when the time length for which the phase error remains between the first and second output levels H and L becomes longer than the reference time length C. Thereafter, the tracking mode is maintained. As previously described, when the amplitude of the phase error of the clock signal remains within the predetermined range for the predetermined period of time in the acquisition mode, the convergence of the phase error is determined, that is, it is determined that the phase of the clock signal shifts close enough to its right phase. Then, the tracking mode begins and the phase of the clock signal is adjusted based on the sampled values of the readout signal obtained at the edge portions thereof, so that the phase thereof is prevented from getting out of a predetermined range in the tracking mode.

FIG. 10 illustrates the switching of the sampled values of the readout signal employed to detect the phase error from the first sampled values S1 to the second sampled values S2. As previously described, the first sampled values S1 output from the ADC 23 are employed to calculate the phase error in the acquisition mode, while the second sampled values S2 output from the EQ 24 are employed in the tracking mode. Although the second sampled values S2 may be employed both in the acquisition and tracking modes, it is desirable to employ the first sampled values S1 in the acquisition mode to quickly adjust the phase of the clock signal. By thus selectively employing the two types of the sampled values S1 and S2 before going through the Viterbi detection circuit 100, the phase of the clock signal can efficiently be controlled with respect to the real sampled values obtained through the PRML method.

However, the first and second sampled values S1 and S2 are employed in parallel with each other to calculate the phase error at one point during the mode switching from the acquisition mode to the tracking mode, due to a delay in outputting the sampled values S2 resulting from the waveform equalization thereon by the EQ 24. As previously described, the sampling conditions of the acquisition and tracking modes differ considerably from each other. Therefore, if the phase error output during the mode switching is employed, the phase of the clock signal may wrongly be adjusted. Hence, according to the present embodiment, the phase error output is masked by the masking signal 46 for a predetermined period of time when the first sampled values S1 are switched to the second sampled values S2. Therefore, the adverse effect of the above delay resulting from the waveform equalization can be eliminated, and the phase of the clock signal is prevented from being wrongly adjusted. According to FIG. 10, the phase error output is masked for a period M, during which the masking signal 46 is supplied. More specifically, the masking signal 46 is supplied from the MPU 28 to the AND circuit 239 shown in FIG. 3 as a gate control signal.

As previously described, the sampled value selection signal 40 switching the sampled value S1 to the sampled value S2 is output from the MPU 28. As shown in FIG. 10, the gain state may be switched from Hi to Low when a certain period of time passes after the switching of the sampled values.

FIG. 11 is a diagram illustrating the normalization of the phase error output. It is desirable to set the gain based on the upper peak (the maximum value) or the lower peak (the minimum value) of the readout signal obtained at the end of the acquisition mode, namely, the amplitude of the

readout signal, so that a gain $K\Phi$ in the transfer function of the clock generation circuit 200 remains constant. By thus adjusting the gain so that the peak-to-peak value of the amplitude of the phase error output remains constant, the readout signal having different amplitudes can be processed without changing the constant of an integrator. The above gain adjustment process is performed by the gain adjustment circuit 238 shown in FIG. 3. In FIG. 11, by being subjected to the above-mentioned gain adjustment process, the peak values of amplitude 500 of the phase error output are reduced to those of amplitude 510 thereof, of which the peak-to-peak value is equal to a predetermined constant peak-to-peak value 520.

The present invention is not limited to the specifically disclosed embodiment, and variations and modifications may be made without departing from the scope of the present invention.

For example, according to the present embodiment, the present invention is applied to the magneto-optical disk as the recording medium. However, the present invention is not limited thereto, and may be applied to any medium from which a signal can be optically read out and to an apparatus having a data reproduction system therefor.

The present application is based on Japanese priority application No. 11-361550 filed on December 20, 1999, the entire contents of which are hereby incorporated by reference.

WHAT IS CLAIMED IS:

1. A clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, said clock adjustment apparatus comprising:

a phase error calculation circuit calculating the phase error of the clock signal based on the sampled values of the readout signal.

2. The clock adjustment apparatus as claimed in claim 1, wherein the readout signal successively comprises a first, a second and a third sampled value in an order sampled, and said phase error calculation circuit calculates the phase error based on a difference between an absolute value of a difference between the first and second sampled values and an absolute value of a difference between the second and third sampled values.

3. The clock adjustment apparatus as

claimed in claim 1, wherein said phase error calculation circuit continuously calculates the phase error based on all of successive sampled values in an acquisition mode in which pattern data having a highest density is reproduced.

4. The clock adjustment apparatus as claimed in claim 1, further comprising:

an edge detection circuit detecting an edge portion of the readout signal based on the transition state of the sampled values of the readout signal,

wherein said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the edge portion of the readout signal detected by said edge detection circuit.

5. The clock adjustment apparatus as claimed in claim 4, wherein:

said edge detection circuit includes a rising edge detection circuit which detects a rising edge portion of the readout signal; and

said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the rising edge portion of the readout signal detected by said rising edge detection circuit.

6. The clock adjustment apparatus as claimed in claim 4, wherein:

said edge detection circuit includes a falling edge detection circuit which detects a falling edge portion of the readout signal; and

said phase error calculation circuit calculates the phase error of the clock signal based on sampled values of the falling edge portion of the readout signal detected by said falling edge detection circuit.

7. The clock adjustment apparatus as claimed in claim 4, wherein said edge detection circuit detects a portion of the readout signal as the edge portion when the portion comprises a series of successive sampled values in ascending order from a value smaller than a predetermined threshold to a value larger than the predetermined threshold, or when the portion comprises a series of successive sampled values in descending order from a value larger than a predetermined threshold to a value smaller than the predetermined threshold.

8. The clock adjustment apparatus as claimed in claim 7, wherein said edge detection circuit detects the portion of the readout signal as the edge portion when the portion comprises a first, a second and a third sampled value in an order sampled with the predetermined threshold being between the first and third sampled values, and a sign of a difference between the first and second

sampled values is equal to that of a difference between the second and third sampled values.

9. The clock adjustment apparatus as claimed in claim 7, wherein:

said edge detection circuit comprises an offset estimation circuit which estimates an offset of the readout signal caused by an envelope variation thereof; and

the predetermined threshold for detecting the edge portion of the readout signal is corrected in accordance with the offset estimated by said offset estimation circuit.

10. The clock adjustment apparatus as claimed in claim 7, further comprising:

a threshold defining circuit defining the predetermined threshold.

11. The clock adjustment apparatus as claimed in claim 4, wherein said phase error calculation circuit operates in an acquisition mode in which the phase error of the clock signal is continuously calculated based on all of successive sampled values of the readout signal and in a tracking mode in which the phase error is calculated based on the sampled values of the edge portion of the readout signal detected by said edge detection

circuit,

said clock adjustment apparatus further comprising an operation mode switching circuit which switches an operation mode of said phase error calculation circuit from the acquisition mode to the tracking mode when an amplitude of the phase error calculated by said phase error calculation circuit remains within a predetermined range for a predetermined period of time in the acquisition mode.

12. The clock adjustment apparatus as claimed in claim 11, wherein said operation mode switching circuit comprises a convergence time setting circuit which sets the predetermined period of time which is used as a reference when switching the operation mode.

13. The clock adjustment apparatus as claimed in claim 11, wherein said operation mode switching circuit comprises a convergence range setting circuit which sets the predetermined range which is used as a reference when switching the operation mode.

14. The clock adjustment apparatus as claimed in claim 11, wherein said phase error calculation circuit comprises a gain adjustment circuit which adjusts a gain according to the phase

error of the clock signal calculated thereby, and employs the adjusted gain to adjust the phase of the clock signal,

said clock adjustment apparatus further comprising a gain switching circuit which sets a first gain with respect to said gain adjustment circuit when said phase error calculation circuit operates in the acquisition mode and a second gain, which is smaller than the first gain, with respect to said gain adjustment circuit when said phase error calculation circuit operates in the tracking mode.

15. The clock adjustment apparatus as claimed in claim 11, wherein:

said data reproduction system comprises an equalizer which performs a waveform equalization on the sampled values of the readout signal; and

said phase error calculation circuit, in the tracking mode, calculates the phase error of the clock signal based on the transition state of the sampled values on which the waveform equalization has been performed by said equalizer.

16. The clock adjustment apparatus as claimed in claim 15, further comprising:

a circuit which prevents the phase of the clock signal from being adjusted based on the phase error calculated by said phase error calculation circuit during a predetermined period of time before and after said phase error calculation circuit

switches from the acquisition mode to the tracking mode.

17. The clock adjustment apparatus as claimed in claim 1, further comprising:

a normalization circuit which normalizes the phase error of the clock signal calculated by said phase error calculation circuit so that a transfer function of a feedback loop for adjusting the phase of the clock signal remains constant.

18. A clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic, said clock adjustment apparatus comprising:

a phase error calculation circuit calculating the phase error of the clock signal based on a transition state of the sampled values of the readout signal before undergoing the Viterbi algorithm.

19. An apparatus comprising:

a data reproduction system which samples a readout signal from a recording medium in synchronism with a clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal, said recording medium being recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic,

said data reproduction system comprising a clock adjustment circuit comprising a phase error calculation circuit calculating a phase error of the clock signal based on the sampled values of the readout signal, and adjusting a phase of the clock signal based on the phase error.

20. The apparatus as claimed in claim 19, wherein the recording medium is formed by an optical disk.

ABSTRACT OF THE DISCLOSURE

A clock adjustment apparatus for adjusting a phase of a clock signal based on a phase error thereof is provided in a data reproduction system which samples a readout signal from a recording medium in synchronism with the clock signal, and reproduces data in accordance with a Viterbi algorithm by using sampled values of the readout signal. The recording medium is recorded with the data modulated in accordance with a recording rule of a predetermined partial response characteristic. The clock adjustment apparatus includes a phase error calculation circuit which calculates the phase error of the clock signal based on the sampled values of the readout signal.

FIG. 1

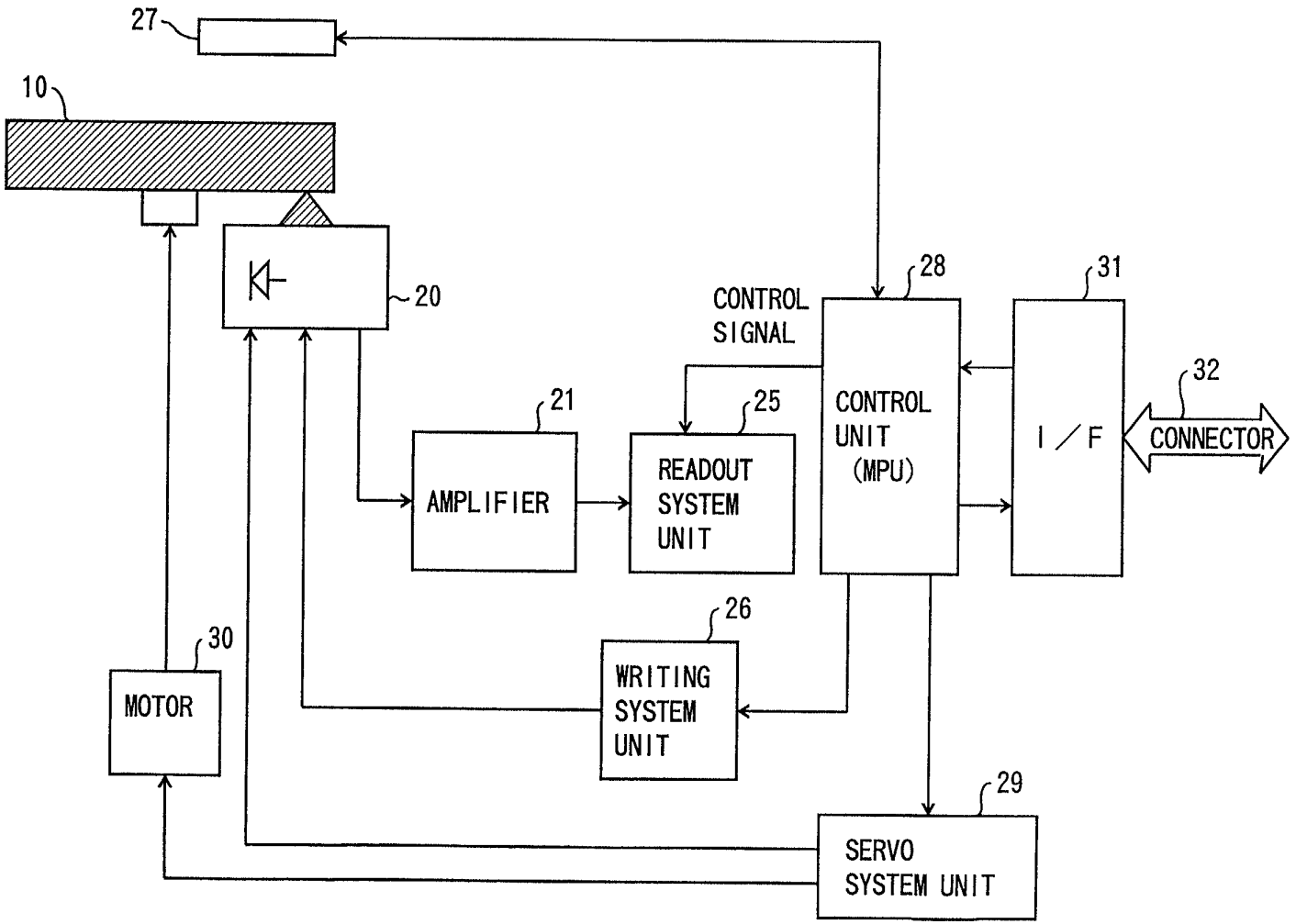

27
10
20
28
31
CONTROL SIGNAL
CONTROL UNIT (MPU)
I／F
32
CONNECTOR
21
AMPLIFIER
25
READOUT SYSTEM UNIT
26
WRITING SYSTEM UNIT
30
MOTOR
29
SERVO SYSTEM UNIT

FIG. 2

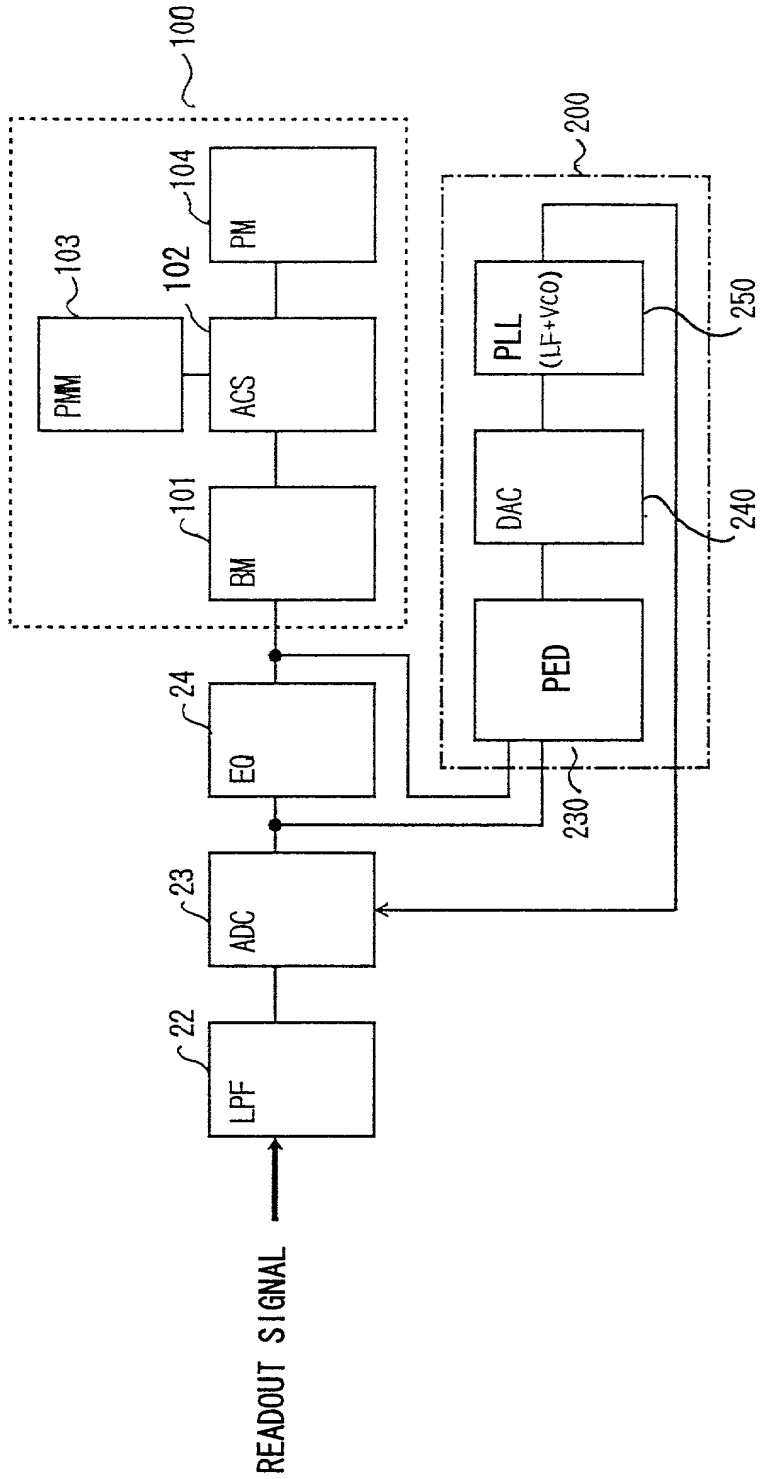

25
100
200
READOUT SIGNAL
LPF
22
ADC
23
EQ
24
BM
101
ACS
102
PMM
103
PM
104
PED
230
DAC
240
PLL
(LF+VCO)
250

FIG. 3

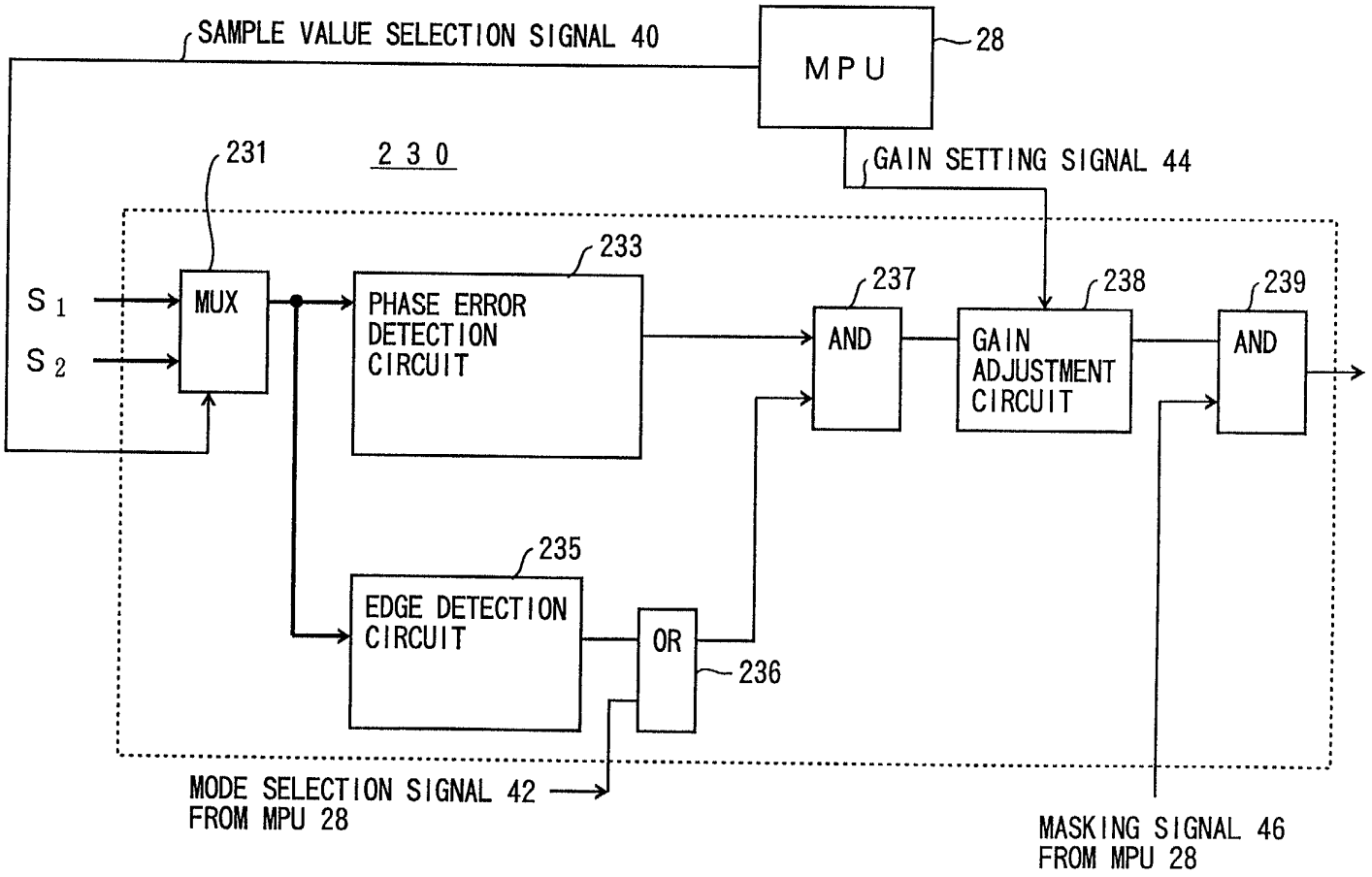
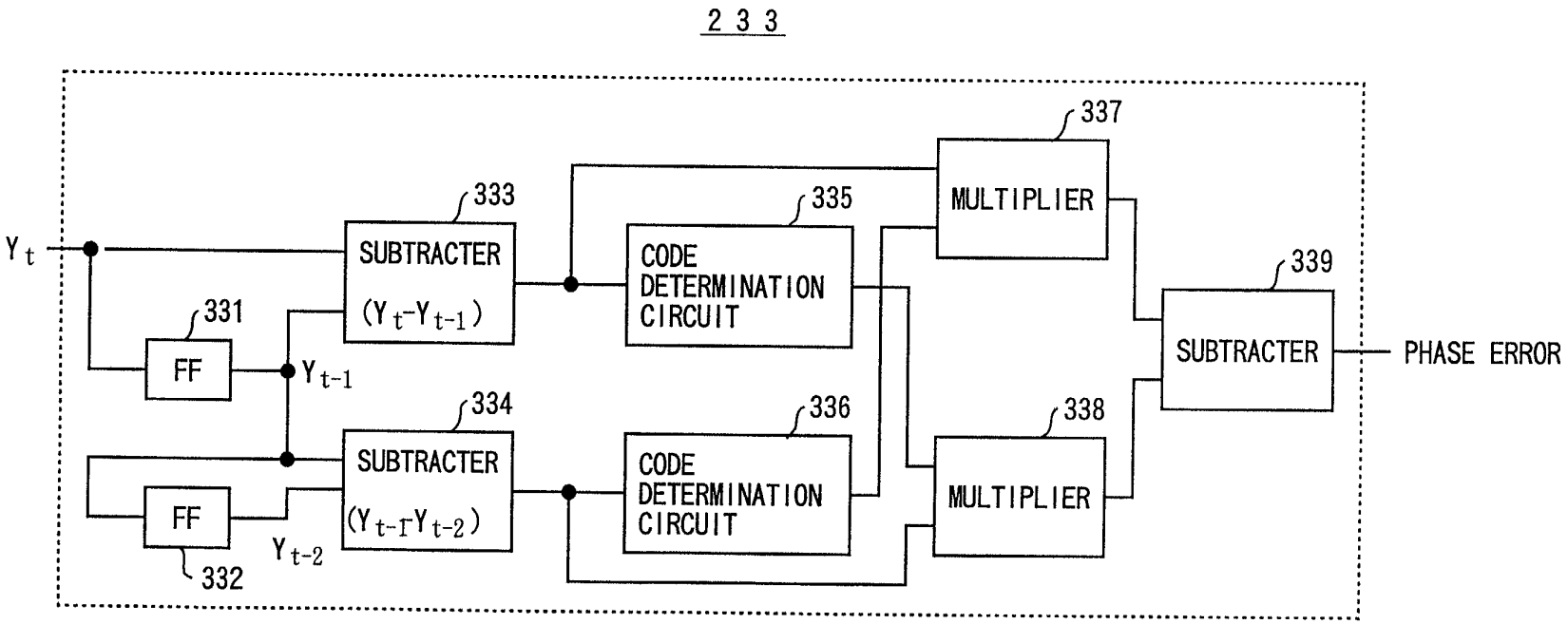

SAMPLE VALUE SELECTION SIGNAL 40
MPU
28
231
230
GAIN SETTING SIGNAL 44
233
237
238
239
S 1
S 2
MUX
PHASE ERROR DETECTION CIRCUIT
AND
GAIN ADJUSTMENT CIRCUIT
AND
235
EDGE DETECTION CIRCUIT
OR
236
MODE SELECTION SIGNAL 42 FROM MPU 28
MASKING SIGNAL 46 FROM MPU 28

FIG. 4


233
337
333
335
MULTIPLIER
Y_t
SUBTRACTER
(Y_t-Y_{t-1})
CODE DETERMINATION CIRCUIT
339
331
SUBTRACTER
PHASE ERROR
FF
Y_{t-1}
334
336
338
SUBTRACTER
$(Y_{t-1}Y_{t-2})$
CODE DETERMINATION CIRCUIT
MULTIPLIER
FF
Y_{t-2}
332

08/08/2008 3:59:59 PM

FIG. 5

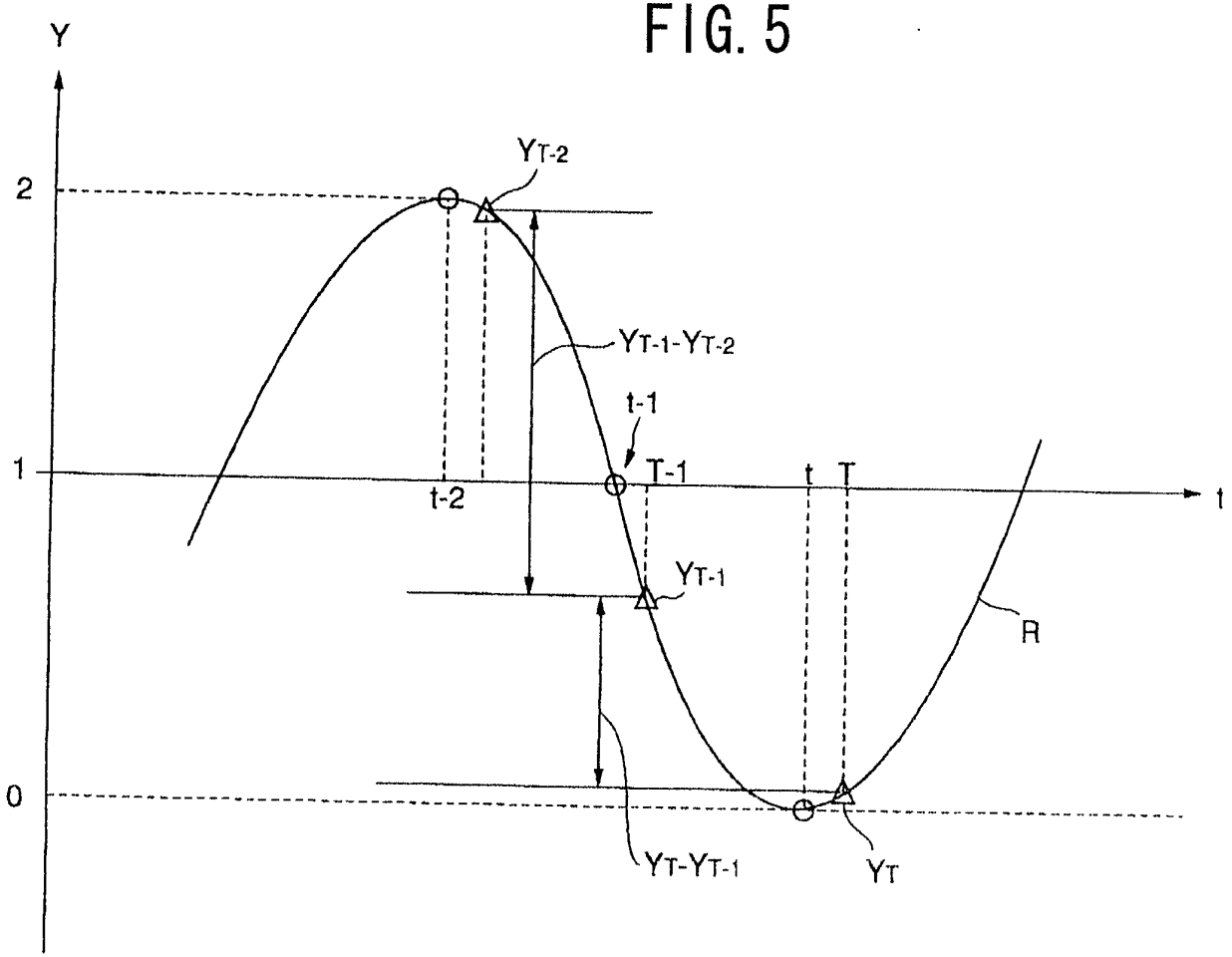
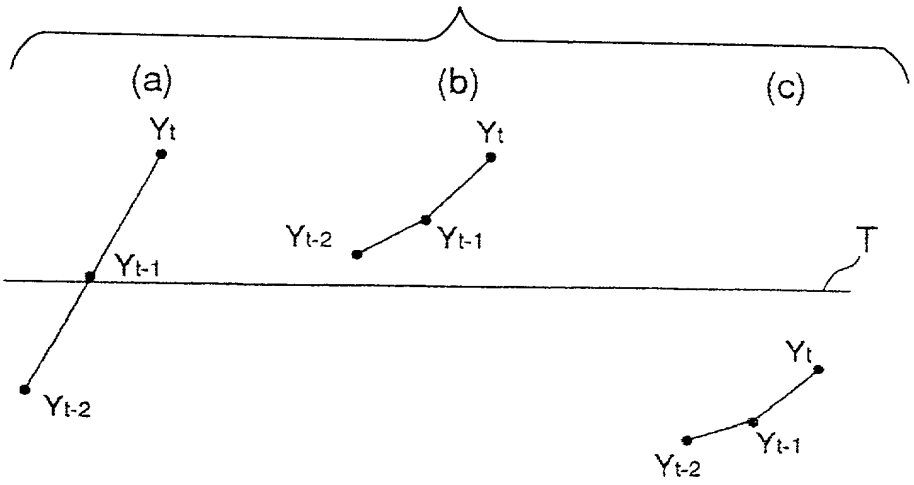


FIG. 6



00206036985960

FIG. 7

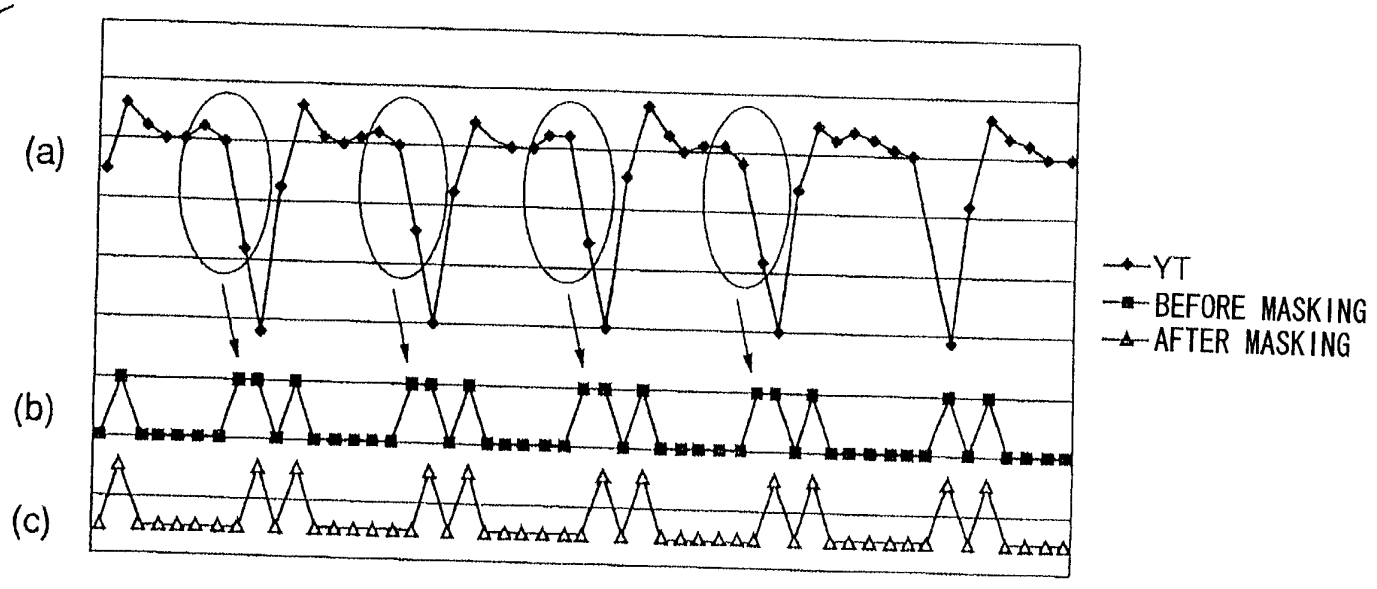


FIG. 8

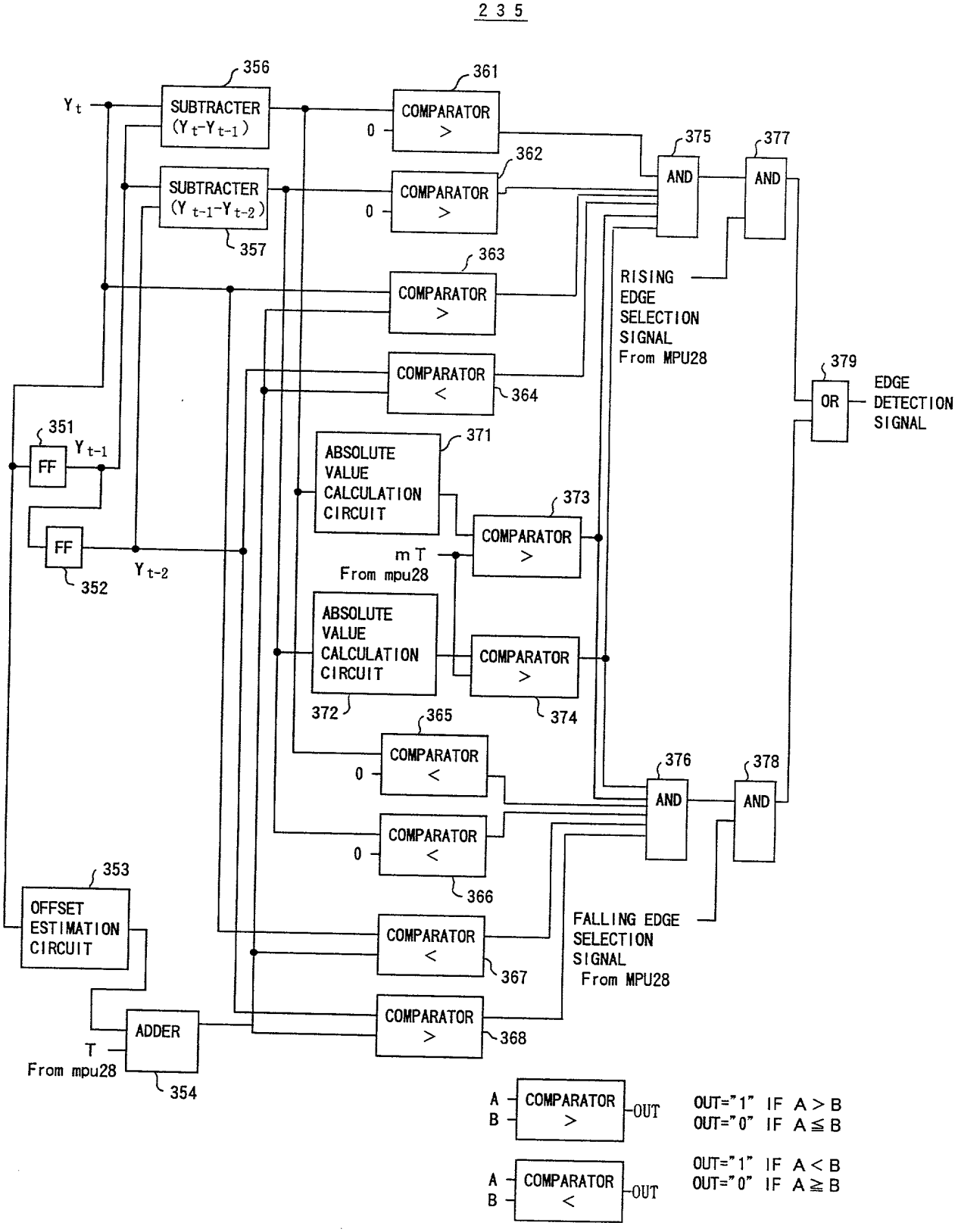

235
356
SUBTRACTER
(Y_t-Y_{t-1})
Y_t
SUBTRACTER
$(Y_{t-1}-Y_{t-2})$
357
361
COMPARATOR
>
0
362
COMPARATOR
>
0
363
COMPARATOR
>
COMPARATOR
<
364
375
AND
377
AND
RISING
EDGE
SELECTION
SIGNAL
From MPU28
379
OR
EDGE
DETECTION
SIGNAL
351
FF
Y_{t-1}
FF
352
Y_{t-2}
371
ABSOLUTE
VALUE
CALCULATION
CIRCUIT
373
COMPARATOR
>
mT
From mpu28
ABSOLUTE
VALUE
CALCULATION
CIRCUIT
372
COMPARATOR
>
374
365
COMPARATOR
<
0
376
AND
378
AND
COMPARATOR
<
0
366
353
OFFSET
ESTIMATION
CIRCUIT
COMPARATOR
<
367
FALLING EDGE
SELECTION
SIGNAL
From MPU28
ADDER
T
From mpu28
354
COMPARATOR
>
368
A
B
COMPARATOR
>
OUT
OUT="1" IF A > B
OUT="0" IF A ≦ B
A
B
COMPARATOR
<
OUT
OUT="1" IF A < B
OUT="0" IF A ≧ B

FIG. 9

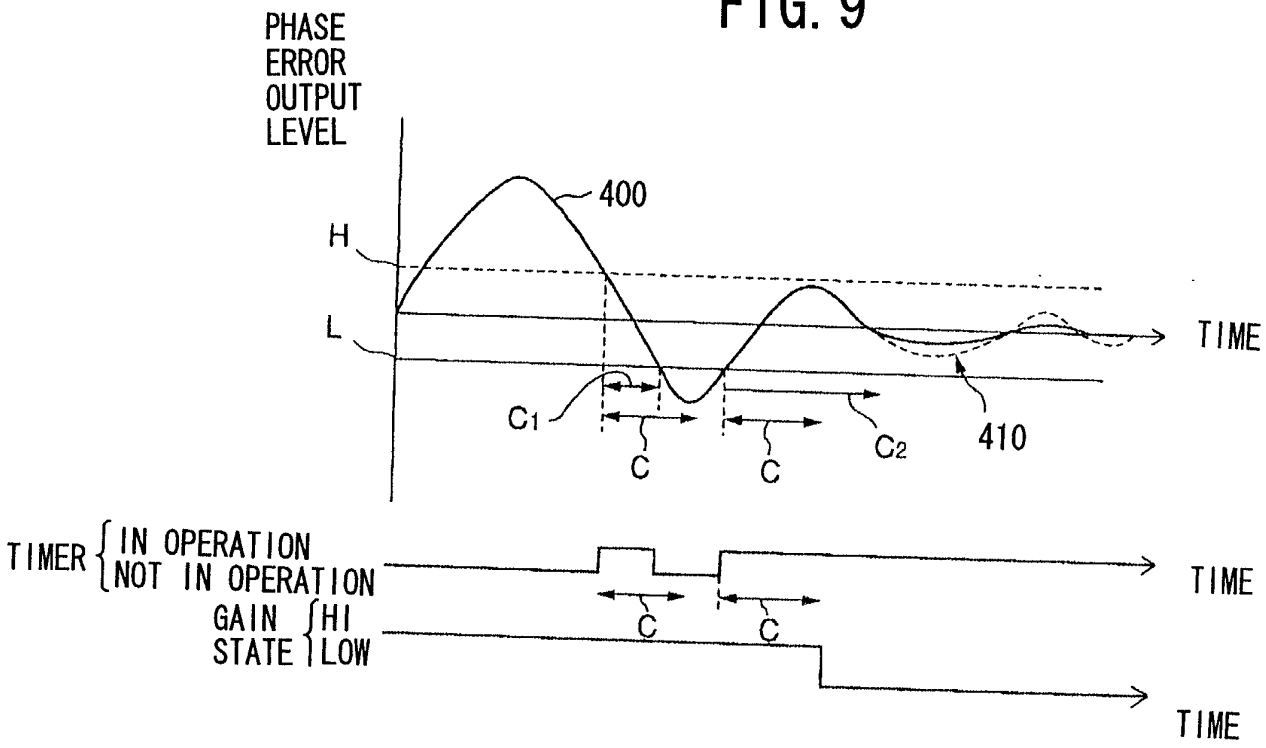

PHASE
ERROR
OUTPUT
LEVEL
400
H
L
TIME
C1
C
C
C2
410
TIMER
IN OPERATION
NOT IN OPERATION
TIME
GAIN
STATE
HI
LOW
C
C
TIME

FIG. 10

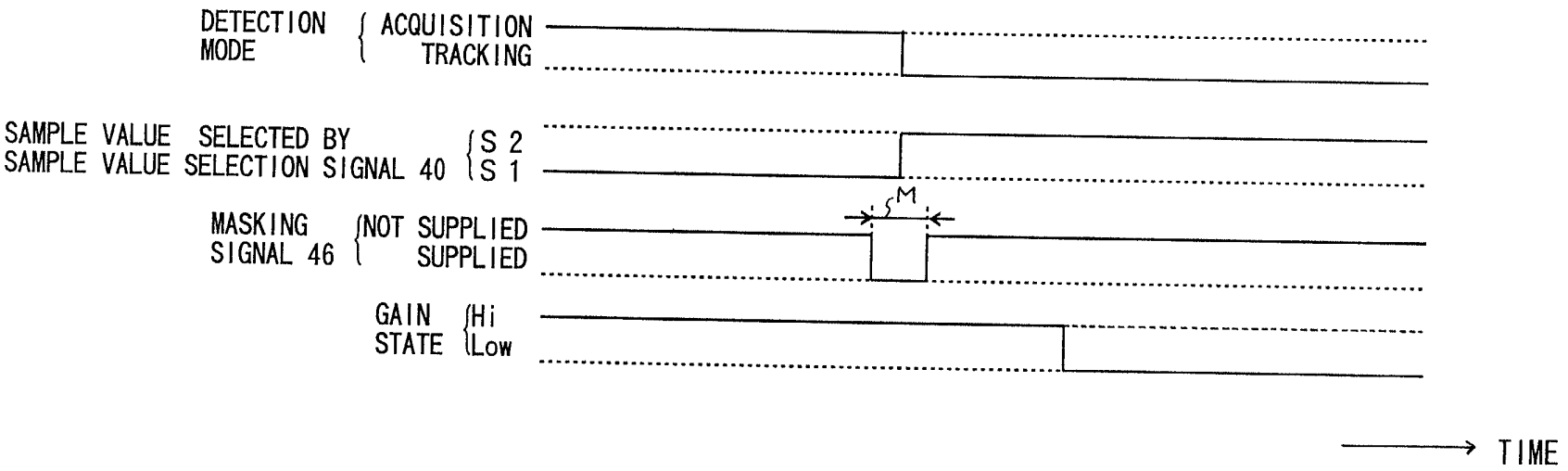
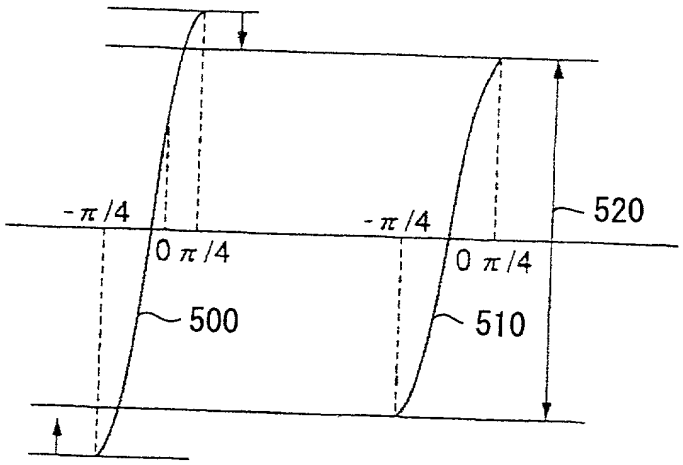

DETECTION MODE
ACQUISITION
TRACKING
SAMPLE VALUE SELECTED BY SAMPLE VALUE SELECTION SIGNAL 40
S 2
S 1
M
MASKING SIGNAL 46
NOT SUPPLIED
SUPPLIED
GAIN STATE
Hi
Low
TIME

FIG. 11



PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CLOCK ADJUSTMENT APPARATUS FOR A DATA REPRODUCTION SYSTEM AND AN APPARATUS HAVING A DATA REPRODUCTION SYSTEM INCLUDING SUCH A CLOCK ADJUSTMENT APPARATUS

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner of Patents and Trademarks, Washington, DC 20231.

PTO/SB/106 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条(a)-(d)項又は３６５条(b)項に基き下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約３６５(a)項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) 外国での先行出願 (Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
Pat. Appln. No.11-361550	Japan	20/December/1999	☐
			☐

☐ 私は、第３５編米国法典１１９条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

☐ I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条(c)に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/108 (8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith *(list name and registration number)*

Attorney	Reg. No.	Attorney	Reg. No.
Patrick G. Burns	29,367	James K. Folker	37,538
Roger D. Greer	26,174	Jonathan D. Feuchtwang	41,017
Lawrence J. Crain	31,497	B. Joe Kim	41,895
Steven P. Fallon	35,132	Joel H. Bootzin	42,343

直接電話連絡先： （名前及び電話番号）

Send Correspondence to:
Direct Telephone Calls to: *(name and telephone number)*

Patrick G. Burns, Esq.
Greer, Burns & Crain, Ltd.
Sears Tower - Suite 8660
Chicago, IL 60606 (312) 993-0080

唯一または第一発明者名	Full name of sole or first inventor Kenichi Hamada
発明者の署名 日付	Inventor's signature Kenichi Hamada Date August 29, 2000
住所	Residence Kawasaki, Japan
国籍	Citizenship Japan
私書箱	Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan
第二共同発明者	Full name of second joint inventor, if any Satoshi Furuta
第二共同発明者 日付	Second inventor's signature Satoshi Furuta Date August 29, 2000
住所	Residence Kawasaki, Japan
国籍	Citizenship Japan
私書箱	Post Office Address c/o FUJITSU LIMITED, 1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan

（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)

Japanese Language Declaration

第3の共同発明者の氏名（該当する場合）	Full name of 3rd joint inventor, if any Masakazu Taguchi
同第3発明者の署名　日付	3rd Inventor's signature　Date Masakazu Taguchi　August 29, 2000
住所	Residence Kawasaki, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address c/o FUJITSU LIMITED,
	1-1, Kamikodanaka 4-chome, Nakahara-ku, Kawasaki-shi, Kanagawa, 211-8588 Japan
第4の共同発明者の氏名（該当する場合）	Full name of 4th joint inventor, if any
同第4発明者の署名　日付	4th Inventor's signature　Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address
第5の共同発明者の氏名（該当する場合）	Full name of 5th joint inventor, if any
同第5発明者の署名　日付	5th Inventor's signature　Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address
第6の共同発明者の氏名（該当する場合）	Full name of 6th joint inventor, if any
同第6発明者の署名　日付	6th Inventor's signature　Date
住所	Residence
国籍	Citizenship
郵便の宛先	Post Office Address

（第7またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for 7th and subsequent joint inventors.)

Form PTO-FB-285 (8-83)
Patent and Trademark Office-U.S. DEPARTMENT OF COMMERCE